



## TFT MODULE SPECIFICATION

### **RVT70HSBFWN00 V1.1A**

EVE4, IPS 7.0" display datasheet  
Rev. 1.0  
2026-05-20

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**Riverdi Sp. z o.o.**

Nowy Swiat 36  
80-299 Gdansk, Poland  
VAT ID: PL5842767153  
Registration number (KRS): 0000923967

**+48 587 703 116**

Office hours: 9:00 to 17:30 CET (Mon-Fri)

**[contact@riverdi.com](mailto:contact@riverdi.com)**

**[riverdi.com](https://riverdi.com)**

| ITEM                           | CONTENTS                                          | UNIT              |
|--------------------------------|---------------------------------------------------|-------------------|
| LCD Type                       | TFT/Transmissive/Normally black/IPS               | /                 |
| Size                           | 7.0                                               | Inch              |
| Viewing Direction              | Free                                              | /                 |
| Outside Dimensions (W x H x D) | 181.60 x 100.60 x 11.80                           | mm                |
| Active Area (W x H)            | 154.21 x 85.92                                    | mm                |
| Pixel Pitch (W x H)            | 0.1506 x 0.1432                                   | mm                |
| Resolution                     | 1024 x 600 (RGB)                                  | /                 |
| Brightness                     | 1000                                              | cd/m <sup>2</sup> |
| Color Depth                    | 16.7 M                                            | /                 |
| Pixel Arrangement              | RGB Vertical Stripe                               | /                 |
| Driver IC of Board             | BT817Q                                            | /                 |
| Rectangular pixel correction   | Yes                                               | /                 |
| Interface                      | SPI/QSPI                                          | /                 |
| QSPI Flash Memory size         | 512                                               | Mb                |
| Host Connector                 | RiBUS, ZIF 20 pin, 0.5mm pitch, down-side contact | /                 |
| With/Without Touch             | Without Touch Panel                               | /                 |
| Supply Voltage for Module      | 3.3                                               | V                 |
| Supply Voltage for Backlight   | 5.0                                               | V                 |
| Audio amplifier                | Build in class-D 1.5W audio amplifier             | /                 |
| Weight                         | TBD                                               | g                 |

**Note 1.** RoHS3 compliant

**Note 2.** LCM weight tolerance: ± 5%.

## 1. REVISION RECORD

| REV NO. | REV DATE   | CONTENTS        | REMARKS |
|---------|------------|-----------------|---------|
| 1.0     | 2026-05-20 | Initial Release |         |

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### 3. MODULE CLASSIFICATION INFORMATION

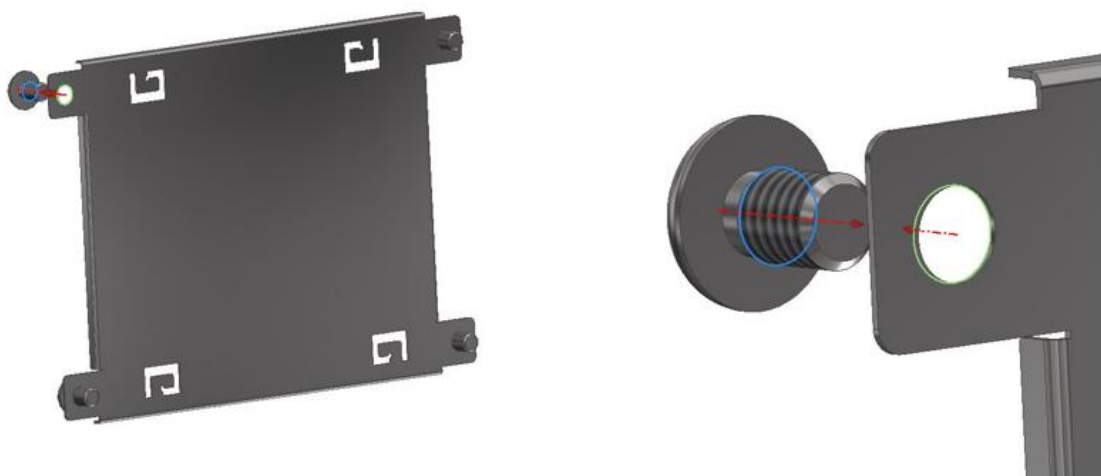
| RV | T  | 70 | H  | S  | B  | F  | W  | N  | 00  | V1.1A |
|----|----|----|----|----|----|----|----|----|-----|-------|
| 1. | 2. | 3. | 4. | 5. | 6. | 7. | 8. | 9. | 10. | 12.   |

| NO. | PARAMETER        | SYMBOL                        |
|-----|------------------|-------------------------------|
| 1.  | BRAND            | RV – Riverdi                  |
| 2.  | PRODUCT TYPE     | T – TFT Standard              |
| 3.  | DISPLAY SIZE     | 70 – 7.0”                     |
| 4.  | MODEL SERIAL NO. | H – High Brightness, IPS      |
| 5.  | RESOLUTION       | S – 1024 x 600 px             |
| 6.  | INTERFACE        | B – SPI/QSPI                  |
| 7.  | FRAME            | F – With Mounting Metal Frame |
| 8.  | BACKLIGHT TYPE   | W – LED White                 |
| 9.  | TOUCH PANEL      | N – Without Touch Panel       |
| 10. | VERSION          | 00 – version                  |
| 11. | MODULE REVISION  | V1.1A                         |

## 4. ASSEMBLY

### 4.1 Mounting Frame

For dimensions 3.5", 4.3", 5.0", 7.0", 10.1" and 12.1" the product with mounting frame version is available. Thanks to the four catches attached to the side, frame provides strong assembly to the surface by mounting element (like the screw, see Figure 1). The frames are specially designed to fit Riverdi products perfectly. The diameter of the mounting hole is 3.5mm.



*Figure 1. Mounting Frame*



## 6. ABSOLUTE MAXIMUM RATINGS

| PARAMETER                                   | SYMBOL   | MIN  | MAX | UNIT |
|---------------------------------------------|----------|------|-----|------|
| Supply Voltage for Module                   | $V_{DD}$ | 0    | 3.6 | V    |
| Digital I/O signals (SPI/QSPI/GPIO) Voltage | -        | -0.5 | 3.3 | V    |
| Supply voltage for Backlight                | BLVDD    | -0.3 | 7.0 | V    |
| Operating Temperature                       | $T_{OP}$ | -20  | 70  | °C   |
| Storage Temperature                         | $T_{ST}$ | -30  | 80  | °C   |

**Note.** The above are maximum values. If exceeded, they may cause permanent damage to the unit.

## 7. ELECTRICAL CHARACTERISTICS

| PARAMETER                 | SYMBOL   | MIN | TYP | MAX | UNIT |
|---------------------------|----------|-----|-----|-----|------|
| Supply Voltage for Module | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V    |
| Input Voltage “H” Level   | $V_{IH}$ | 2.0 | -   | 3.3 | V    |
| Input Voltage “L” Level   | $V_{IL}$ | -   | -   | 0.8 | V    |

| PARAMETER                   | SYMBOL    | MIN | TYP | MAX | UNIT | NOTE   |
|-----------------------------|-----------|-----|-----|-----|------|--------|
| Current drawn from VDD@3.3V | $I_{VDD}$ | -   | TBD | TBD | mA   | Note 1 |

**Note 1.** Animated pictures are displayed on the screen and there is no QSPI communication during the measurement of TYP and MAX values.

TYP value is measured when the audio is off.

MAX value is measured when the audio is on, and volume is set to maximum.

Riverdi loudspeaker RVA-SPK1.5W-C150 is applied during the measurement.

## 8. BACKLIGHT ELECTRICAL CHARACTERISTICS

| PARAMETER                    | SYMBOL | MIN | TYP    | MAX | UNIT  | NOTE   |
|------------------------------|--------|-----|--------|-----|-------|--------|
| Supply Voltage for Backlight | BLVDD  | 4.5 | 5.0    | 5.5 | V     | Note 1 |
| Lifetime                     | -      | -   | 50.000 | -   | Hours | Note 2 |

**Note 1.** The Min voltage of BL driver is 2.7V, the modules will work, but full brightness can't be achieved.

**Note 2.** Operating life means the period in which the LED brightness goes down to 50% of the initial brightness. Typical operating lifetime is the estimated parameter.

| PARAMETER                      | SYMBOL      | MIN BL | 50% BL | 100% BL | UNIT | NOTE   |
|--------------------------------|-------------|--------|--------|---------|------|--------|
| Current drawn from BLVDD @4.5V | $I_{BLVDD}$ | TBD    | TBD    | TBD     | mA   | Note 3 |
| Current drawn from BLVDD @5.0V | $I_{BLVDD}$ | TBD    | TBD    | TBD     |      |        |
| Current drawn from BLVDD @5.5V | $I_{BLVDD}$ | TBD    | TBD    | TBD     |      |        |

**Note 3.** To control the backlight dimming, please refer to subchapter 11.4.

MIN BL is when REG\_PWM\_DUTY = 1

50% BL is when REG\_PWM\_DUTY = 64

100% BL is when REG\_PWM\_DUTY = 128

## 9. ELECTRO-OPTICAL CHARACTERISTICS

| ITEM                       | SYMBOL   | CONDITION                                      | MIN   | TYP   | MAX   | UNIT              | RMK    | NOTE |
|----------------------------|----------|------------------------------------------------|-------|-------|-------|-------------------|--------|------|
| Response Time              | Tr+Tf    | $\theta=0^\circ$<br>$\phi=0^\circ$<br>Ta=25 °C | -     | 28    | 45    | ms                | FIG 2. | 4, 7 |
| Contrast Ratio             | Cr       |                                                | 600   | 800   | -     | ---               | FIG 3. | 1, 7 |
| Surface Luminance          | Lv       |                                                | -     | 1000  | -     | cd/m <sup>2</sup> |        | 2, 7 |
| Viewing Angle Range        | $\theta$ | $\phi = 90^\circ$                              | 80    | 85    | -     | deg               | FIG 4. | 6    |
|                            |          | $\phi = 270^\circ$                             | 80    | 85    | -     | deg               |        |      |
|                            |          | $\phi = 0^\circ$                               | 80    | 85    | -     | deg               |        |      |
|                            |          | $\phi = 180^\circ$                             | 80    | 85    | -     | deg               |        |      |
| CIE (x, y)<br>Chromaticity | Rx       | $\theta=0^\circ$<br>$\phi=0^\circ$<br>Ta=25 °C | 0.581 | 0.611 | 0.641 | -                 | FIG 3. | 5,7  |
|                            | Ry       |                                                | 0.295 | 0.325 | 0.355 | -                 |        |      |
|                            | Gx       |                                                | 0.306 | 0.336 | 0.366 | -                 |        |      |
|                            | Gy       |                                                | 0.513 | 0.543 | 0.573 | -                 |        |      |
|                            | Bx       |                                                | 0.117 | 0.148 | 0.178 | -                 |        |      |
|                            | By       |                                                | 0.127 | 0.157 | 0.187 | -                 |        |      |
|                            | Wx       |                                                | 0.291 | 0.321 | 0.351 | -                 |        |      |
|                            | Wy       |                                                | 0.315 | 0.345 | 0.375 | -                 |        |      |
| Uniformity                 | U        |                                                | 70    | 75    | -     | %                 | Fig 3. |      |
| NTSC ratio                 | -        | -                                              | 40    | 47    | -     | %                 |        |      |

**Note 1.** Contrast Ratio (CR) is defined mathematically as below, for more information see Figure 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

**Note 2.** Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

$L_v$  = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

**Note 3.** The uniformity in surface luminance  $\delta$  WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of 5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 2.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

**Note 4.** Response time is the time required for the display to transition from white to black (Rise Time,  $T_r$ ) and from black to white (Decay Time,  $T_f$ ). For additional information see Figure 1. The test equipment is BM-7A.

**Note 5.** CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then make average value.

**Note 6.** For TFT module, viewing angle is the angle at which the contrast ratio is greater 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 3.

**Note 7.** Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80). For response time testing, the testing data is based on BM-7A. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, Chromaticity the test data is based on SR-3A.

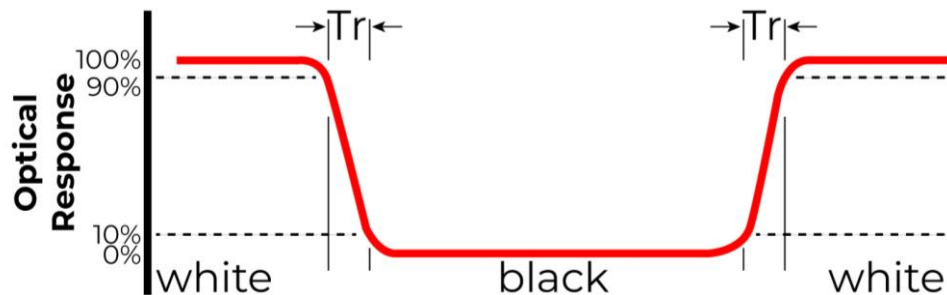


Figure 2. The definition of response time

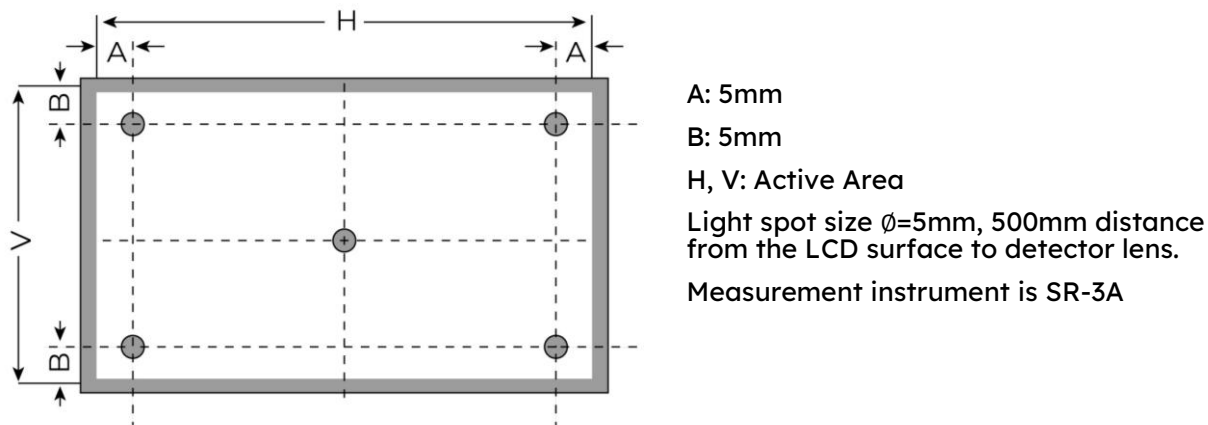


Figure 3. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity

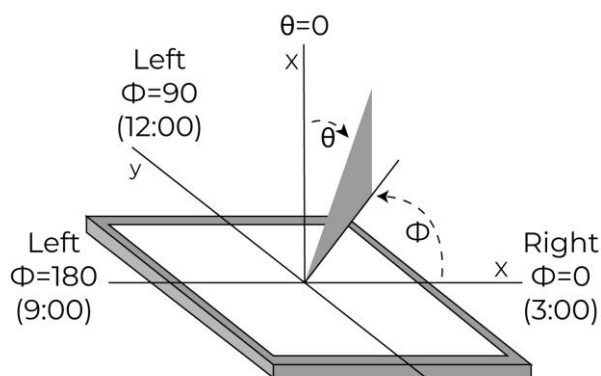


Figure 4. The definition of viewing angle

## 10. INTERFACES DESCRIPTION

### 10.1 P1 connector – RiBUS description

| PIN          | SYMBOL      | DESCRIPTION                                                                    |
|--------------|-------------|--------------------------------------------------------------------------------|
| <b>1</b>     | VDD         | Supply voltage for module; TYP 3.3 V                                           |
| <b>2</b>     | GND         | Ground                                                                         |
| <b>3</b>     | SPI_SCLK    | SPI SCK signal                                                                 |
| <b>4</b>     | MISO/ IO.1  | SPI MISO signal / SPI Quad mode: SPI data line 1                               |
| <b>5</b>     | MOSI/ IO.0  | SPI MOSI signal / SPI Quad mode: SPI data line 0                               |
| <b>6</b>     | CS          | SPI chip select signal                                                         |
| <b>7</b>     | INT         | Interrupt signal from device to the system, Active Low, internally 47k Pull UP |
| <b>8</b>     | RST/PD      | Reset / Power down signal, Active Low, Internally Pulled UP 47k                |
| <b>9</b>     | GPIO.0      | GPIO.0                                                                         |
| <b>10</b>    | DISP_AUDIO  | Display audio in/out                                                           |
| <b>11</b>    | GPIO.1/IO.2 | SPI Single/Dual mode: General purpose IO0.<br>QSPI mode: SPI data line 2       |
| <b>12</b>    | GPIO.2/IO.3 | SPI Single/Dual mode: General purpose IO1.<br>QSPI mode: SPI data line 3       |
| <b>13-16</b> | NC          | Not connected                                                                  |
| <b>17</b>    | BLVDD       | Supply voltage for backlight                                                   |
| <b>18</b>    | BLVDD       | Supply voltage for backlight                                                   |
| <b>19</b>    | BLGND       | Backlight Ground, internally connected to GND                                  |
| <b>20</b>    | BLGND       | Backlight Ground, internally connected to GND                                  |

## 10.2 P2 connector description – AUDIO interface description

| PIN | SYMBOL   | DESCRIPTION               |
|-----|----------|---------------------------|
| 1   | SPEAKER+ | Speaker coil “+” terminal |
| 2   | SPEAKER- | Speaker coil “-” terminal |

The audio circuit allows for the following 3 modes:

1. To play sounds from BT817Q on internal amplifier U3.
2. To play sounds from host on internal amplifier U3.
3. To play sounds from BT817Q on external amplifier.

**Note 1.** Matched Riverdi louder speaker for all EVE4 series displays: RVA-SPK1.5W-C150

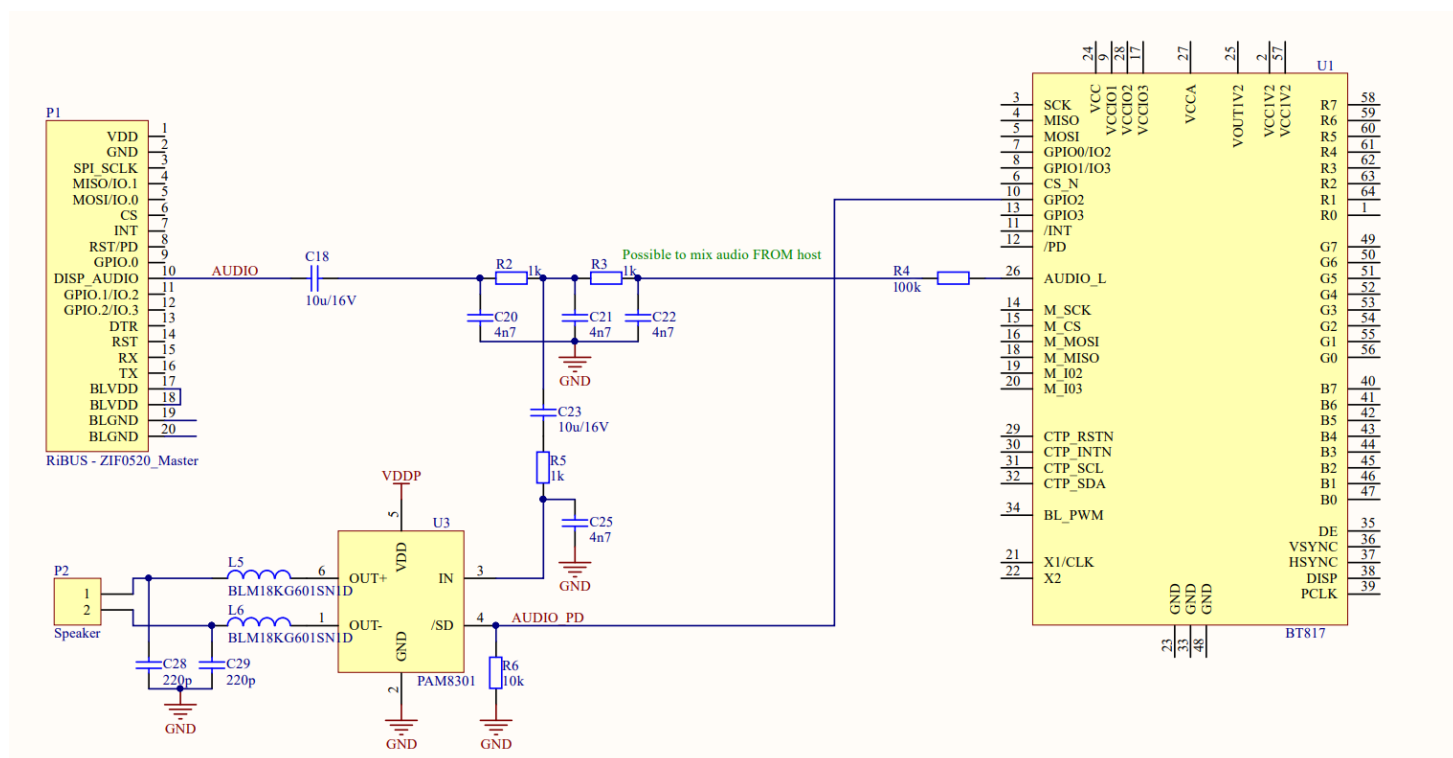


Figure 5. The simplified audio circuit design

## 11. BT817Q CONTROLLER SPECIFICATION

BT817Q or EVE4 (Embedded Video Engine 4) simplifies the system architecture for advanced human machine interfaces (HMIs) by providing functionality for display, audio, and touch as well as an object-oriented architecture approach that extends from display creation to the rendering of the graphics.

### 11.1 Serial host interface

Figure 6. SPI single/dual interface connection

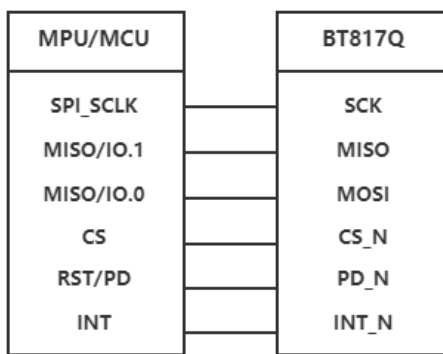
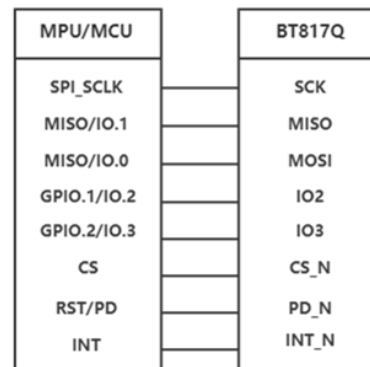


Figure 7. QSPI interface connection



**SPI Interface** – the SPI slave interface operates up to 30MHz.

Only SPI mode 0 is supported. The SPI interface is selected by default.

**QSPI Interface** – the QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported.

The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.

By default, the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG\_SPI\_WIDTH.

## 11.2 Block diagram

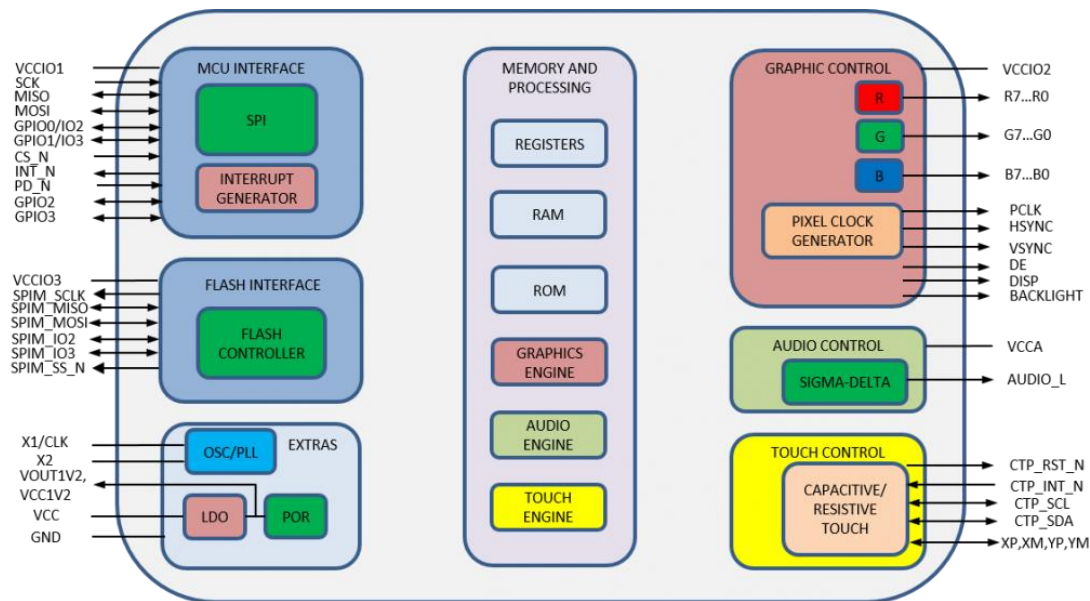


Figure 8. BT817Q Block diagram

## 11.3 Host interface SPI mode 0

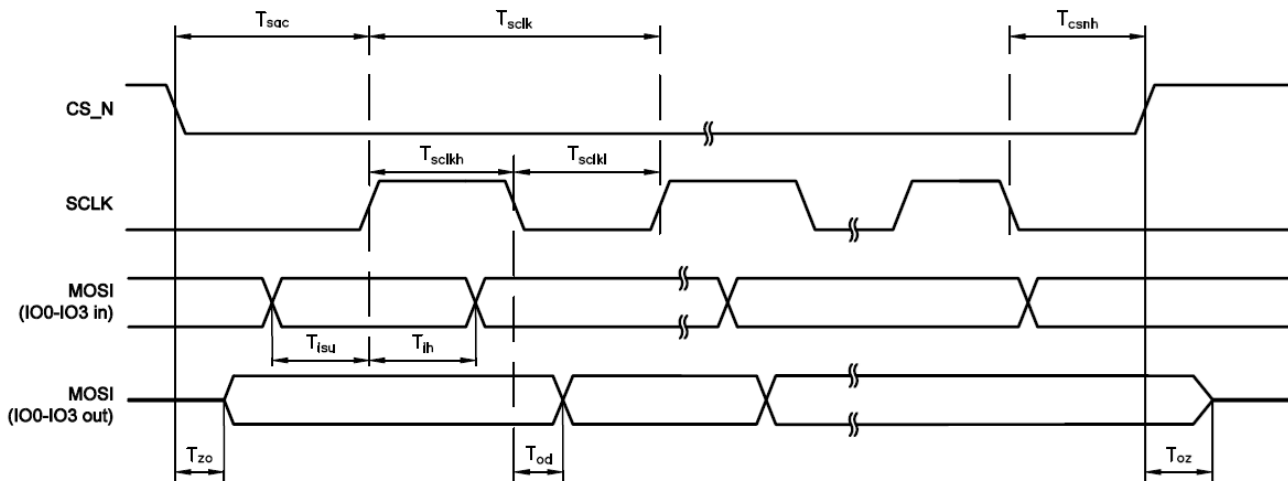


Figure 9. SPI timing diagram

The meanings of the timings in the Figure 9 are defined in the table below.

| PARAMETER          | DESCRIPTION             | VCCIO=1.8V |     | VCCIO=2.5V |     | VCCIO=3.3V |     | UNIT |
|--------------------|-------------------------|------------|-----|------------|-----|------------|-----|------|
|                    |                         | MIN        | MAX | MIN        | MAX | MIN        | MAX |      |
| T <sub>sclk</sub>  | SPI clock period        | 33.3       | -   | 33.3       | -   | 33.3       | -   | ns   |
| T <sub>scld</sub>  | SPI clock low duration  | 13         | -   | 13         | -   | 13         | -   | ns   |
| T <sub>scldh</sub> | SPI clock high duration | 13         | -   | 13         | -   | 13         | -   | ns   |
| T <sub>sac</sub>   | SPI access time         | 4          | -   | 3.5        | -   | 3          | -   | ns   |
| T <sub>isu</sub>   | Input Setup             | 4          | -   | 3.5        | -   | 3          | -   | ns   |
| T <sub>ih</sub>    | Input Hold              | 0          | -   | 0          | -   | 0          | -   | ns   |
| T <sub>zo</sub>    | Output enable delay     | -          | 16  | -          | 13  | 11         | -   | ns   |
| T <sub>oz</sub>    | Output disable delay    | -          | 13  | -          | 11  | 10         | -   | ns   |
| T <sub>od</sub>    | Output data delay       | -          | 15  | -          | 12  | 11         | -   | ns   |
| T <sub>csnh</sub>  | CSN hold time           | 0          | -   | 0          | -   | 0          | -   | ns   |

For more information about BT817Q controller please go to official BT81x website.

<https://brtchip.com/product/bt817/>

## 11.4 Backlight driver block diagram

Backlight enable signal is internally connected to BT817Q backlight control pin. This pin is controlled by two BT817Q's registers. **REG\_PWM\_HZ** specifies the PWM output frequency. The recommend PWM backlight frequency ranges from 10kHz to 100kHz.

**REG\_PWM\_DUTY** specifies the duty cycle.

Refer to BT817Q datasheet for more information.

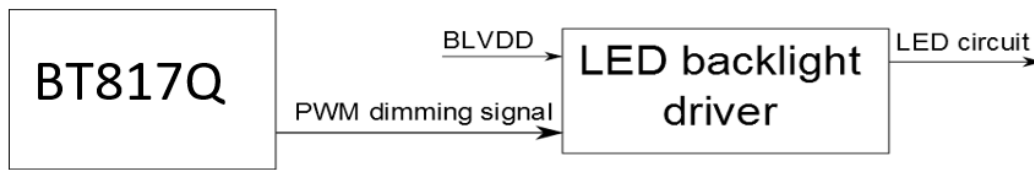


Figure 10. Backlight driver block diagram

The LED backlight driver used in this module does not burst the LED current. Therefore, it does not generate audible noises on the output capacitor. It is equipped with soft start subsystem, which increases LED lifetime, as LED current peaks are reduced significantly.

## 12. 512MB NOR FLASH MEMORY

The Riverdi EVE4 7.0" series modules are built with a 512Mb NOR flash memory chip. Graphics assets such as fonts, audio, and images can be stored in the flash memory. Up to 170 full resolution (1024 \* 600 pixels, JPG) images can be stored. If you need to change the memory size, please contact: [contact@riverdi.com](mailto:contact@riverdi.com)

There is an additional port P3 for programming the flash memory directly from an external source. This port is designed to be used during production if the customer wants to order pre-programmed EVE4 boards with graphic content of their own choice.

Cable TC2050-IDC-NL is compatible with P3 programming port

## 13. TFT LCD TIMING CHARACTERISTICS

The TFT of module applies Riverdi high brightness, IPS, 7.0" RGB TFT: RVT70HSTFWN00

For detailed information of the display, please refer to datasheet of display.

### 13.1 Parallel RGB timing characteristics

#### 13.1.1 Horizontal input timing

| PARAMETER                           | SYMBOL           | MIN  | TYP  | MAX  | UNIT |
|-------------------------------------|------------------|------|------|------|------|
| Horizontal display area             | thd              | 1024 |      |      | DCLK |
| DCLK frequency<br>(frame rate 60Hz) | f <sub>clk</sub> | 44.9 | 51.2 | 63   | MHz  |
| 1 Horizontal Line                   | t <sub>h</sub>   | 1200 | 1344 | 1400 | DCLK |

|                   |           |     |     |     |      |
|-------------------|-----------|-----|-----|-----|------|
| HSYNC pulse width | $t_{hpw}$ | 1   | -   | 140 | DCLK |
| HSYNC back porch  | $t_{hbp}$ | 160 | 160 | 160 | DCLK |
| HSYNC front porch | $t_{hfp}$ | 16  | 160 | 216 | DCLK |

### 13.1.2 Horizontal input timing

| PARAMETER             | SYMBOL    | MIN | TYP | MAX | UNIT |
|-----------------------|-----------|-----|-----|-----|------|
| Vertical display area | $t_{vd}$  | 600 |     |     | H    |
| VSYNC period time     | $t_v$     | 624 | 635 | 750 | H    |
| VSYNC pulse width     | $t_{vpw}$ | 1   | -   | 20  | H    |
| VSYNC back porch      | $t_{vb}$  | 23  | 23  | 23  | H    |
| VSYNC front porch     | $t_{vfp}$ | 1   | 12  | 127 | H    |

## 14. MODULE INITIALIZATION

1. There is no need to set touch calibration matrix (REG\_TOUCH\_TRANSFORM\_A-F registers in BT817Q) as touch panel resolution and orientation are the same as display, so default values in BT817Q are correct.
2. Initialization data, timings and example codes are available on the Riverdi GitHub, at address: <https://github.com/riverdi/riverdi-eve>
3. REGISTER VALUES:

| PARAMETER   | SYMBOL |
|-------------|--------|
| REG_HSIZE   | 1024   |
| REG_VSIZE   | 600    |
| REG_HCYCLE  | 1344   |
| REG_HOFFSET | 160    |
| REG_HSYNC0  | 0      |
| REG_HSYNC1  | 70     |

|               |              |
|---------------|--------------|
| REG_VCYCLE    | 635          |
| REG_VOFFSET   | 23           |
| REG_VSYNC0    | 0            |
| REG_VSYNC1    | 10           |
| REG_PCLK      | 1            |
| REG_SWIZZLE   | 0            |
| REG_PCLK_POL  | 1            |
| REG_CSPREAD   | 0            |
| REG_DITHER    | 0            |
| REG_PCLK_FREQ | 3346 (0xD12) |
| REG_PCLK_2X   | 0            |

## 15. INSPECTION

Standard acceptance/rejection criteria for TFT module according to document available [here](#).

## 16. RELIABILITY TEST

| NO. | TEST ITEM                           | TEST CONDITION                                                                                                                                 | NOTE      |
|-----|-------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| 1   | High Temperature Storage            | 80°C/120 hours                                                                                                                                 | A,B,C,D,E |
| 2   | Low Temperature Storage             | -30°C/120 hours                                                                                                                                |           |
| 3   | High Temperature Operating          | 70 °C /120 hours                                                                                                                               |           |
| 4   | Low Temperature Operating           | -20°C/120 hours                                                                                                                                |           |
| 5   | High Temperature and High Humidity  | Humidity 60°C, 90%RH, 120Hrs                                                                                                                   |           |
| 6   | Thermal Cycling Test (No operation) | -20°C for 30min, 70°C for 30 min.<br>100 cycles. Start with cold and end with high temperature.                                                | A,B,C,D,E |
| 7   | Vibration Test                      | Sweep:10Hz~55Hz~10Hz 2G<br>2 hours for each direction of X. Y. Z.<br>(6 hours for total)                                                       | A,B,C,D,E |
| 8   | Package vibration test              | Random Vibration:<br>0.015G*G/Hz from 5-200HZ, -<br>6dB/Octave from 200-500HZ<br>2 hours for each direction of X. Y. Z.<br>(6 hours for total) | A,B,C,D,E |
| 9   | Package Drop Test                   | Height: 60 cm<br>1 corner, 3 edges, 6 surfaces                                                                                                 | A,B,C,D,E |
| 10  | ESD                                 | Contact=+/-2KV, Air=+/-<br>4KV,(R=330R,C=150pF), 1<br>sec,9point,10times/point;                                                                | A,B,C,D,E |

### Note.

A.LCM each function is OK.

B.LCM appearance inspection without abnormalities (Including scratch, damage, corrosion and serious deformation)

C.LCM brightness above the Min. value of Spec.

D. Luminance uniformity above the Min. value of Spec.

E. Color chromaticity within tolerance range

## 17. LEGAL INFORMATION

CE marking is usually obligatory only for a complete end product. Riverdi display modules are semi-finished goods which are used as inputs to become part of the finished products.

Therefore, Riverdi display modules are not CE marked.

This is not a standalone product. It was designed as an electronic component. It needs integration with a whole system to be fully functional.

Riverdi grants the guarantee for the proper operation of the goods for a period of 12 months from the date of possession of the goods. If in a consequence of this guaranteed execution the customer has received the defects-free item as replacement for the defective item, the effectiveness period of this guarantee shall start anew from the moment the customer receives the defects-free item.

Information about device is the property of Riverdi and may be the subject of patents pending or granted. It is not allowed to copy or disclosed this document without prior written permission.

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## 18. CONTACT

### Your Success is Our Priority

Stuck on a technical challenge? Need expert guidance?  
Our dedicated support team is just a message away.

Contact us at

[\*\*contact@riverdi.com\*\*](mailto:contact@riverdi.com)

We're here to ensure your project's success, every step of the way!